

1   **What is claimed is:**

2           1.    A strained silicon carbon alloy MOSFET structure,  
3   comprising:

4           a substrate;  
5           a graded SiGe layer on the substrate;  
6           a relaxed buffer layer on the graded SiGe layer;  
7           a strained silicon carbon alloy layer on the relaxed  
8                buffer layer acting as a channel;  
9           a gate dielectric layer on the strained layer;  
10          a polysilicon gate electrode on the gate dielectric  
11                layer; and  
12          a source and drain region on the substrate opposite and  
13                adjacent to the polysilicon gate electrode.

1           2.    The structure of claim 1, wherein the relaxed  
2   buffer layer comprises Si-Ge-C alloy, Si, Ge or other  
3   combinations of at least two semiconductor materials.

1           3.    The structure of claim 1, wherein the gate  
2   dielectric layer comprises  $\text{HfO}_2$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{Al}_2\text{O}_3$ , or any high  
3   dielectric constant (high k) dielectric material.

1           4.    The structure of claim 1, wherein the MOSFET is a  
2   NMOS or PMOS.

1           5.    The structure of claim 1, wherein the gate  
2   dielectric layer comprises Al, Pt, TaN, TiN, or any metal  
3   gate dielectric.

1        6.    The structure of claim 1, wherein the gate  
2 polysilicon layer comprises poly-SiGe.

1        7.    The structure of claim 5, wherein the gate  
2 polysilicon layer comprises n-type or p-type dopants.

1        8.    The structure of claim 1, wherein the substrate  
2 comprises n-type and p-type doped Ge, III-V group  
3 semiconductor, or silicon-on-insulator (SOI).

4        9.    A method of strained silicon carbon alloy MOSFET  
5 fabrication, comprising the steps of:  
6        forming a graded SiGe layer on a substrate;  
7        forming a relaxed buffer layer on the graded SiGe  
8        layer;  
9        forming a strained silicon carbon alloy layer on the  
10       relaxed buffer layer acting as a channel;  
11       forming an gate dielectric layer on the strained  
12       silicon carbon alloy layer;  
13       forming a gate polysilicon layer on the gate dielectric  
14       layer;  
15       etching the gate dielectric layer and the gate  
16       polysilicon layer to form a polysilicon gate  
17       electrode with a sidewall spacer; and  
18       forming a source/drain region on the substrate opposite  
19       and adjacent to the polysilicon gate electrode.

1        10.   The method of claim 9, wherein the relaxed buffer  
2 layer comprises Si-Ge-C alloy, Si, Ge or other combinations  
3 of at least two semiconductor materials.

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1        11. The method of claim 9, wherein the gate dielectric  
2 layer comprises  $\text{HfO}_2$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{Al}_2\text{O}_3$ , or any high dielectric  
3 constant (high k) dielectric material.

1        12. The method of claim 9, wherein the MOSFET is a  
2 NMOS or PMOS.

1        13. The structure of claim 9, wherein the gate  
2 dielectric layer comprises Al, Pt, TaN, TiN, or any metal  
3 gate dielectric.

4        14. The method of claim 9, wherein the gate  
5 polysilicon layer comprises poly-SiGe.

1        15. The method of claim 14, wherein the gate  
2 polysilicon layer comprises n-type or p-type dopants.

1        16. The method of claim 9, wherein the substrate  
2 comprises n-type and p-type doped Ge, III-II group  
3 semiconductor, or silicon-on-insulator (SOI).